



PONTIFICIA UNIVERSIDAD CATOLICA DE CHILE  
ESCUELA DE INGENIERIA  
DEPARTAMENTO DE CIENCIA DE LA COMPUTACION

**Complexity Theory, Semester I 2017 - IIC3242**

**Homework 6**

Deadline: Sunday, 18th of June, 2017

## 1 The majority gate [4 points + 1 bonus point]

Here we define a new type of a gate to be used in circuits called a *majority gate*. A majority gate takes  $n$  inputs  $x_1, \dots, x_n$  (that is, the fan-in is unbounded), and returns the value  $(\sum_{i=1}^n x_i) \geq \frac{n}{2}$ . That is, it returns 1 if and only if at least half of the inputs have the value 1.

In this task you are asked to show that the parity function  $P_n$  which evaluates to 1 iff the number of input values that are equal 1 is odd (see the slides for circuit complexity) can be computed by circuits that use only the majority gate and the negation gate. You do not need to draw any circuits if you do not feel so inclined. A simple description will do. A small hint: for this you do not really need to consider the parity function, but show something much more general. What could that be? (Remember that we already know how to compute parity.)

For a bonus point show that this can be done in constant depth and polynomial size.

## 2 Probabilistic SAT [3 points]

Show that, if  $\text{NP} \subseteq \text{BPP}$ , then there is a probabilistic polynomial time algorithm that constructs a satisfying assignment for a formula  $\varphi \in \text{SAT}$  with probability at least  $\frac{1}{2}$  and rejects when a formula is not satisfiable.

Hint: you can use a BPP algorithm for SAT that has error probability of  $2^{-|\varphi|}$  and try to use the same idea as in self-reducibility of SAT (see classes on circuit complexity). The main part of the proof is to show that the probability is at least  $\frac{1}{2}$ .